

WHAT IS CLAIMED IS:

1 1. A logic circuit comprising:

2 a dynamic logic portion for evaluating a Boolean function of a plurality of
3 data input signals, wherein a logic signal on a dynamic node asserted in response to a
4 first logic state of a clock signal comprises either a logic true or a logic false Boolean
5 combination of the plurality of the data input signals and the dynamic node is pre-
6 charged to a first logic state corresponding to the logic false Boolean combination
7 when the clock signal has a second logic state;

8 a static portion having a pull-down input, a data input coupled to the dynamic
9 node, a data output node generating a latched data output signal in response to the
10 logic signal and the clock signal, and an inverted data output node generating a
11 latched inverted data output signal as the logic inversion of the latched data output
12 signal, wherein the inverted data output node is set to a logic zero when the pull-down
13 input is a logic one and the inverted data output node is held at a logic zero when the
14 data output signal is a logic one; and

15 a feedforward pulse circuit having a first input coupled to the dynamic node, a
16 second input coupled to the inverted data output node, and a pulse node coupled to
17 the pull-down input and generating a feedforward pulse, wherein the feedforward
18 pulse is a logic one when the dynamic node is a logic zero and the inverted data
19 output signal is a logic one.

1 2. The logic circuit of claim 1, wherein the dynamic logic portion comprises:

2 a first P channel field effect transistor (PFET) having a gate terminal coupled
3 to the clock signal, a source terminal coupled to a positive power supply voltage and a
4 drain terminal coupled to the dynamic node, wherein the dynamic node is coupled to
5 the positive power supply voltage in response to the first logic state of the clock
6 signal and isolated from the positive power supply voltage in response to a second
7 logic state of the clock signal;

8 a logic tree having a plurality of logic inputs, a positive tree terminal coupled
9 to the dynamic node, and a negative tree terminal, wherein the positive tree terminal
10 is coupled to the negative tree terminal in response to first logic states of the plurality
11 of logic inputs and isolated from the negative tree terminal in response to second
12 logic states of the plurality of logic inputs; and

13 a first N channel FET (NFET) having a gate terminal coupled to the clock
14 signal, a drain terminal coupled to the negative tree terminal and a source terminal
15 coupled to a negative power supply voltage, wherein the negative tree terminal is
16 coupled to the negative power supply voltage in response to the second logic state of
17 the clock signal and isolated from the negative power supply voltage in response to a
18 first logic state of the clock signal.

1 3. The logic of claim 1 wherein the static portion comprises:

2 a first PFET having a gate coupled to the dynamic node, a source coupled to
3 the first power supply voltage and a drain;

4 a first NFET having a gate coupled to the gate of the first PFET, a drain
5 coupled to the drain of the first PFET for a data output node generating the data
6 output signal, and a source;

7 a second NFET having a gate coupled to the second clock signal, a source
8 coupled to the second power supply voltage and a drain coupled to the source of the
9 first NFET;

10 a third NFET having a drain coupled to the drain of the second NFET, a
11 source coupled to the second power supply voltage and a gate;

12 an inverting circuit having an input coupled to the data output node and an
13 output coupled to the inverted data output node;

14 a fourth NFET having a source coupled to the second power supply voltage, a
15 drain coupled to the inverted data output node, and a gate coupled to the pull-down
16 input; and

17 and a second PFET having a gate coupled to the output node of the inverting
18 circuit, a drain coupled to the data output node and a source coupled to the first power
19 supply voltage.

1 4. The logic circuit of claim 1, wherein the feedforward pulse circuit comprises:
2 a first NFET having a source coupled to the second power supply voltage, a
3 drain and a gate coupled to the dynamic node;
4 a first PFET having a drain coupled to the drain of the first NFET forming the
5 pulse node, a gate coupled to the dynamic node and a source;
6 a second PFET having a drain coupled to the source of the first PFET, a
7 source coupled to the first power supply voltage and a gate; and
8 an inverter having an input coupled to the inverted data output node, and
9 output coupled to the gate of the first PFET.

1 5. The logic circuit of claim 3, wherein the inverting circuit comprises:
2 a third PFET having a gate coupled to the data output node, a source coupled
3 to the first power supply voltage and a drain; and
4 a fifth NFET having a gate coupled to the gate of the third PFET, a source
5 coupled to the second power supply voltage and a drain coupled to the drain of the
6 third PFET forming the inverted data output node.

1 6. The logic circuit of claim 5, wherein the fourth NFET is substantially larger
2 than the fifth NFET.

1 7. The logic circuit of claim 6, wherein the fourth NFET is about ten times larger
2 than the fifth NFET.

1 8. The logic circuit of claim 6, wherein all PFETs and all NFETs in a logic path
2 driving the fifth NFET may be made smaller when the fourth NFET is made
3 substantially larger than the fifth NFET.

1 9. A data processing system comprising:

2 a central processing unit (CPU); and

3 a memory operable for communicating instructions and operand data to the
4 CPU which includes a logic system having a logic circuit with a dynamic logic
5 portion for evaluating a Boolean function of a plurality of data input signals, wherein
6 a logic signal on a dynamic node asserted in response to a first logic state of a clock
7 signal comprises either a logic true or a logic false Boolean combination of the
8 plurality of the data input signals and the dynamic node is pre-charged to a first logic
9 state corresponding to the logic false Boolean combination when the clock signal has
10 a second logic state, a static portion having a pull-down input, a data input coupled to
11 the dynamic node, a data output node generating a latched data output signal in
12 response to the logic signal and the clock signal, and an inverted data output node
13 generating a latched inverted data output signal as the logic inversion of the latched
14 data output signal, wherein the inverted data output node is set to a logic zero when
15 the pull-down input is a logic one and the inverted data output node is held low when
16 the data output signal is a logic one; and a feedforward pulse circuit having a first
17 input coupled to the dynamic node, a second input coupled to the inverted data output
18 node, and a pulse node coupled to the pull-down input and generating a feedforward
19 pulse, wherein the feedforward pulse is a logic one when the dynamic node is a logic
20 zero and the inverted data output signal is a logic one.

1 10. The data processing system of claim 9, wherein the dynamic logic portion
2 comprises:

3 a first P channel field effect transistor (PFET) having a gate terminal coupled
4 to the clock signal, a source terminal coupled to a positive power supply voltage and a
5 drain terminal coupled to the dynamic node, wherein the dynamic node is coupled to
6 the positive power supply voltage in response to the first logic state of the clock
7 signal and isolated from the positive power supply voltage in response to a second
8 logic state of the clock signal;

9 a logic tree having a plurality of logic inputs, a positive tree terminal coupled
10 to the dynamic node, and a negative tree terminal, wherein the positive tree terminal
11 is coupled to the negative tree terminal in response to first logic states of the plurality
12 of logic inputs and isolated from the negative tree terminal in response to second
13 logic states of the plurality of logic inputs; and

14 a first N channel FET (NFET) having a gate terminal coupled to the clock
15 signal, a drain terminal coupled to the negative tree terminal and a source terminal
16 coupled to a negative power supply voltage, wherein the negative tree terminal is
17 coupled to the negative power supply voltage in response to the second logic state of
18 the clock signal and isolated from the negative power supply voltage in response to a
19 first logic state of the clock signal.

1 11. The data processing system of claim 9 wherein the static portion comprises:

2 a first PFET having a gate coupled to the dynamic node, a source coupled to
3 the first power supply voltage and a drain;

4 a first NFET having a gate coupled to the gate of the first PFET, a drain
5 coupled to the drain of the first PFET for a data output node generating the data
6 output signal, and a source;

7 a second NFET having a gate coupled to the second clock signal, a source
8 coupled to the second power supply voltage and a drain coupled to the source of the
9 first NFET;

10 a third NFET having a drain coupled to the drain of the second NFET, a
11 source coupled to the second power supply voltage and a gate;

12 an inverting circuit having an input coupled to the data output node and an
13 output coupled to the inverted data output node;

14 a fourth NFET having a source coupled to the second power supply voltage, a
15 drain coupled to the inverted data output node, and a gate coupled to the pull-down
16 input; and

17 and a second PFET having a gate coupled to the output node of the inverting
18 circuit, a drain coupled to the data output node and a source coupled to the first power
19 supply voltage.

1 12. The data processing system of claim 9, wherein the feedforward pulse circuit
2 comprises:

3 a first NFET having a source coupled to the second power supply voltage, a
4 drain and a gate coupled to the dynamic node;

5 a first PFET having a drain coupled to the drain of the first NFET forming the
6 pulse node, a gate coupled to the dynamic node and a source;

7 a second PFET having a drain coupled to the source of the first PFET, a
8 source coupled to the first power supply voltage and a gate; and

9 an inverter having an input coupled to the inverted data output node, and
10 output coupled to the gate of the first PFET.

1 13. The data processing system of claim 11, wherein the inverting circuit
2 comprises:

3 a third PFET having a gate coupled to the data output node, a source coupled
4 to the first power supply voltage and a drain; and

5 a fifth NFET having a gate coupled to the gate of the third PFET, a source
6 coupled to the second power supply voltage and a drain coupled to the drain of the
7 third PFET forming the inverted data output node.

1 14. The data processing system of claim 13, wherein the fourth NFET is
2 substantially larger than the fifth NFET.

1 15. The data processing system of claim 14, wherein the fourth NFET is about ten
2 times larger than the fifth NFET.

1 16. The logic circuit of claim 14, wherein all PFETs and all NFETs in a logic path
2 driving the fifth NFET may be made smaller when the fourth NFET is made
3 substantially larger than the fifth NFET.